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Dynamic voltage restorer using multi cascaded H-Bridge with a dual control strategy to Energy self-recovery and fault Current Limiting

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Abstract: - In this paper, a cascaded H-Bridge dynamic voltage restorer system is proposed to improve the voltage quality of sensitive loads using two control strategies. The existing control strategies either put emphasis on the optimal control during steady operation stage of voltage compensation or correct the phase angle jump in the initial stage of voltage compensation. Recently, the impact of phase jump characteristic of voltage sag on the load side after voltage sag recoveries is widely ignored, further, there are still drawbacks in existing energy self-recovery strategies of DVR. Therefore, to improve the overall voltage compensation time while correcting the phase jump and accelerate the energy recovery of dc link side, this project aims to 1) Propose the strategies to minimum active power consumption during voltage compensation stage and maximum active power absorption during energy self-recovery stage. 2) Deliver smooth transition in dynamic process to ensure the flexible switching between two stages. Additionally, proposed system can perform short circuit current limiting function by activating anti-parallel thyristors during short circuit fault and deactivating them during normal operation. Theoretical analysis of proposed strategy is been validated through simulation results.

Key Words— ***DVR, Cascaded H-Bridge, Dual control strategy***

I. INTRODUCTION

In recent years, different aspects of the DVR have been studied [12]-[19]. The typical topology of DVR is as shown in Fig. 1.1 [12]-[13], which is mainly composed of an energy storage system or an alternative power source, a voltage source converter, an output filter and a coupling transformer. The voltage sag issue is commonly associated with a phase jump characteristic in the load side voltage waveform [19]. Further, the value of phase angle jump may be increased by energy-optimized compensation strategies [14]. The phase jump issues worth deep studies because it causes the voltage flicker and may lead to extreme transient currents in the electrical power units such as capacitors, transformers, and motors [20]. These issues were noticed and combined with the DVR's control to make corresponding improvements in [21]. However, the energy in the DC link capacitor continues to be consumed in voltage compensation stage, then, the enhancement of compensation time is limited. An enhanced scheme is proposed in [22]. It mitigates the phase jump in the early stage of compensation and enhances the sag compensation time at the same time.

An adaptive scheme proposed in this paper features the following superiorities and operational characteristics:

- The initial operating point of recovery process should be adjusted according to the final state of voltage compensation to avoid any further phase angle jump after fault removal. The perfect linkage between recovery operation and voltage compensation is designed.
- The DC link voltage after the voltage sag disappearance is recovery to the set value promptly, which ensure the equipment ready for the next compensation. Meanwhile, the injected voltage will not perturb the magnitude and phase angle of load voltage during.

II. METHODOLOGY

A. Self-recovery control scheme

Owing to the randomness of voltage sag, U_S and U_L are measured in real time. Under normal condition, the DVR works in stand-by mode. The voltage compensation stage is initiated while $k_{sag} > k_{ref} = 0.05$. Then, the operation mode and the operating point are determined based on the values of k_{sag} and $\cos(\theta_L)$. Further, once the amplitude of U_{DVR} bigger than

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the given value U_{DVRmax}, the injected voltage angle during the voltage compensation stage and energy self-recovery stage is regulated thus avoiding overmodulation. Fig. 10 depicts the detailed block diagram of the proposed comprehensive scheme. To realize the voltage compensation, the vital step involves obtaining the reference injected voltage angle of DVR. The phase calculation block computes the phase angle θ_{DVRf} and $\theta_{DVRi.}$ Then, the DVR injection angle is obtained through the transition 1 and transition 2. Similarly, to realize the energy self-recovery, the vital step involves obtaining the value of γ. Then, the DVR injection angle is obtained through the transition 3 and transition 2. The DVR reference voltage U_{DVRref} or U_{injref} is obtained and compared with the actual voltage in the stationary reference frame. A proportional integral (PI) controller is used for accurate tracking of U_{DVRref} or U_{injref}. After SPWM modulation technology is applied, the driving signal of IGBT is obtained [27]. Further, the energy exchange between super-capacitor and C_{dc} is done by DC/DC converter, and the detailed control strategy has been described in [28] already.

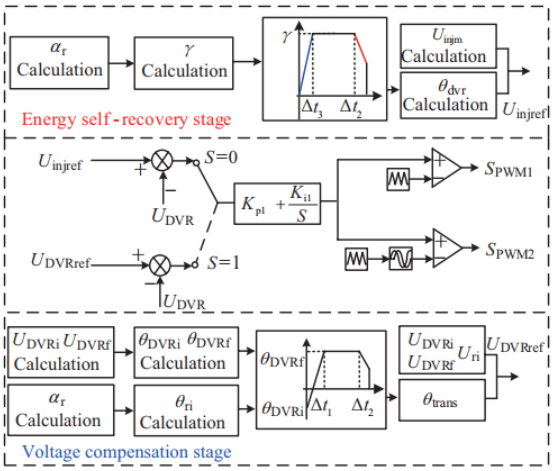

Fig. 1: Control strategy of DVR for voltage compensation and energy self-recovery.

III. Fault Current Limiting Control Scheme

When the MCDVR operates in the fault current limiting mode, the fault current will flow through the series transformer *T*1, *LC* output filter, and the bidirectional thyristors. The series transformer withstands the supply voltage during the faults, and hence the capacity of the series transformer is

$$S_T \geq U_s I_{fault} \qquad (1)$$

In addition, the thermal stability of *Lf*, and the maximal withstand voltage of C*f* should be considered during the faults. This relation is expressed as:

$$Q_{Lf} \geq \int_{t_{fault}}^{t_{return}} (k i_{fault})^2 \qquad (2)$$

where Q_{Lf} is the thermal stability of L_f during the fault. t_{fault} and t_{return} are the time of the fault occurring and disappearing respectively. As the filter capacitor can be easily damaged by the overvoltage,

$$U_{Cf} \geq \max(u_{s\max}/k, u_{dc}) \qquad (3)$$

where U_{Cf} is the maximal withstand voltage of the filter capacitor. u_{dc} and u_{Smax} are the dc voltage and the maximum voltage across the series transformer respectively. When the thyristors are deactivated, the voltages between the thyristors are the same as the output voltage of the cascade converter. The maximum value of the output voltages is approximately equal to the DC side voltage, while the current flowing through the thyristors is zero. When the thyristors are activated during the fault, the current flowing through the thyristor is *k* times of the fault current at the primary side. Thus, the thyristors can be given by

$$Q_{thy} \geq \int_{t_{fault}}^{t_{return}} (k i_{fault})^2 dt \qquad (4)$$

$$U_{thy} \geq \max(u_{cf}, u_{dc}) \qquad (5)$$

Ride-through capability:

Assuming that the magnitude of the voltage sag (with no phase-angle jump) is U_{sag} in pu, the MCDVR should inject an active power given by

$$P_{DVR} = -C_{dc} u_{dc} du_{dc}/dt = \sqrt{3} U_L I_L \cos\theta_L (1 - U_{sag}) \qquad (6)$$

to restore the pre-sag rated voltage *U*L at the load terminals [14]. Here, the load current *I*L and the power factor φL are assumed to be constant. Furthermore, $P_L = \sqrt{3} U_L I_L \cos\phi_L$ is the rated load power. If *t*sag is the voltage sag duration, the energy to be supplied by the MCDVR is

$$W_{DVR} = \int_{t_0}^{t_0+t_{sag}} (-C_{dc} u_{dc} \frac{du_{dc}}{dt}) = \int_{t_0}^{t_0+t_{sag}} P_L (1 - U_{sag}) dt \qquad (7)$$

Then,

$$-C_{dc}[u_{dc}^2(t_0 + t_{sag}) - u_{dc}^2(t_0)]/2 = P_L t_{sag}(1 - U_{sag}) \qquad (8)$$

If the initial dc-link voltage is assumed to be its rated value, then *u*dc(t0)=*U*dc0. *u*dc(t0+tsag)=*k*d*U*dc0 where *k*d*U*dc0 is

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the minimum allowable dc-link voltage at the end of the voltage sag ($0<k_d<1$). Thus, in order to compensate the maximum voltage sag magnitude for a maximum expected sag duration $U_{sag,max}$, the capacitance should be

$$C_{dc} \geq 2P_L t_{sag,\max}(1-U_{sag,\max})/u_{dc0}^2(1-k_d^2) \qquad (9)$$

increasing U_{dc0} allows the reduction of the size of the dc capacitor, but the choice of that voltage also depends on the maximum voltage rating of the H-bridge power electronic devices. Furthermore, the capacitor voltage rating also limits the maximum injection voltage. Two balancing schemes are adopted [28], and are not discussed in this paper for brevity.

IV. Proposed System And Results

The typical topology of DVR is as shown in Fig. 2 [12]-[13], which is mainly composed of an energy storage system or an alternative power source, a voltage source converter, an output filter and a coupling transformer.

The voltage sag issue is commonly associated with a phase jump characteristic in the load side voltage waveform [19]. Further, the value of phase angle jump may be increased by energy-optimized compensation strategies [14]. The phase jump issues worth deep studies because it causes the voltage flicker and may lead to extreme transient currents in the electrical power units such as capacitors, transformers, and motors [20]. These issues were noticed and combined with the DVR's control to make corresponding improvements in [21]. However, the energy in the DC link capacitor continues to be consumed in voltage compensation stage, then, the enhancement of compensation time is limited. An adaptive scheme proposed in this paper features the following superiorities and operational characteristics:

- The initial operating point of recovery process should be adjusted according to the final state of voltage compensation to avoid any further phase angle jump after fault removal. The perfect linkage between recovery operation and voltage compensation is designed.
- The DC link voltage after the voltage sag disappearance is recovery to the set value promptly, which ensure the equipment ready for the next compensation. Meanwhile, the injected voltage will not perturb the magnitude and phase angle of load voltage during the whole recovery operation stage.

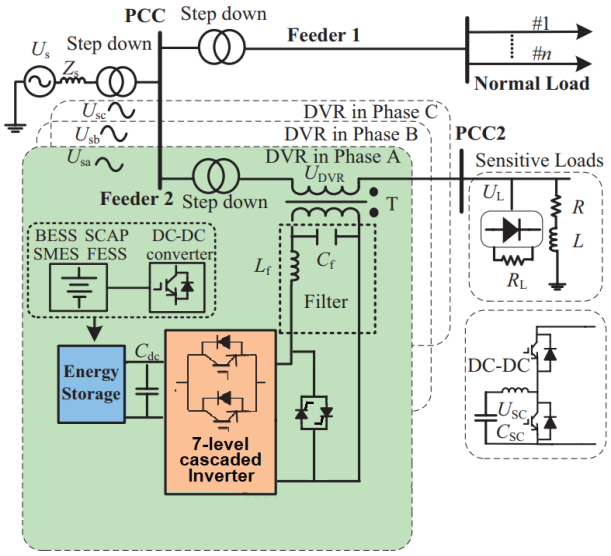

Fig. 2. Typical topology of DVR-based system.

In this section, a MATLAB/SIMULINK model in single phase as shown in Fig.5.1 is built, and the performance of proposed control scheme is validated for various sag cases. The system performance is carried out using solver 23 tb in variable step with a sample time of 20 μs.

Fig.3 show the simulation waveforms in voltage compensation stage using the proposed strategy. In Fig. 3, the system voltage drops to 0.8 p.u. during 0.2~0.3 s. The result shows that the DVR with flexible switching control can smoothly enter and exit the state of minimum energy compensation, which ensure negligible phase angle jump to the load voltage.

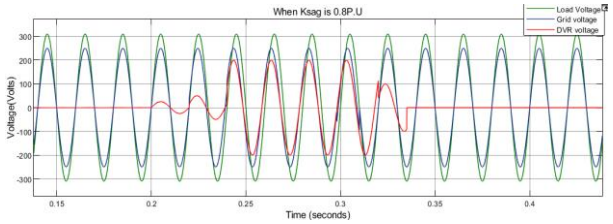

Fig. 3. Simulation waveforms of when *k*sag is 0.8 p.u.

A. Simulation Results During Energy Self-Recovery Stage

In this case, the energy self-recovery operation of DVR is executed. The reference value of *U*dc and *U*DVRmax is set to 300 V and 250 V respectively. To verify the effectiveness of the energy self-recovery strategy presented in this paper, the reference value of *U*SC is changed from 50 V to 60 V. The values of 1.414 *U*rf is calculated as 189 V using (8). Hence, as can be seen from Fig. 5.4, the energy self-recovery stage is initiated at 0.40 s.

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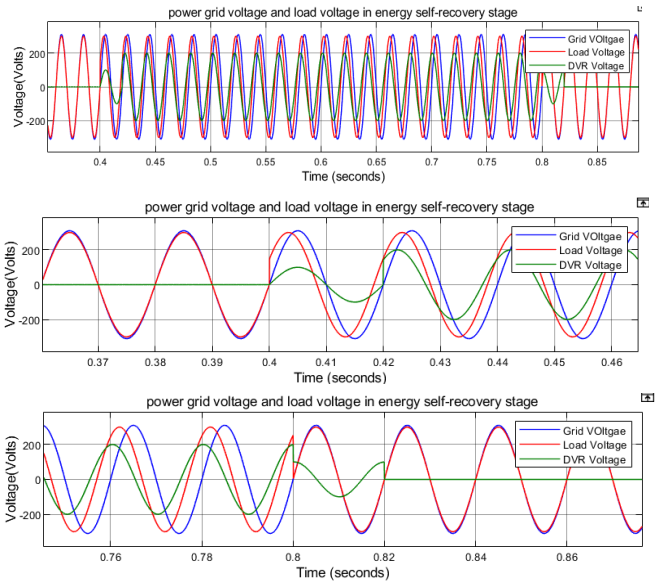

Fig. 4. Simulation waveforms of power grid voltage and load voltage in optimal energy self-recovery stage.

B. Simulation Results During Energy Self-Recovery Stage Using Optimized Strategy

The simulation scenario is same as the condition mentioned above. With the introduction of θtrans3 and θtrans2, the amplitude of *U*L is always consistent with *U*S as can be seen in Fig.5. and Fig.6.

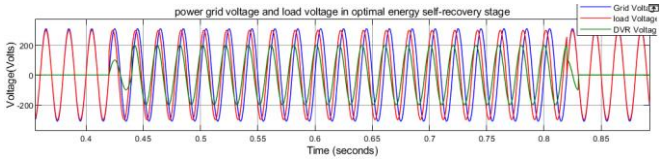

Fig.5. Simulation waveforms of power grid voltage and load voltage in optimal energy self-recovery stage.

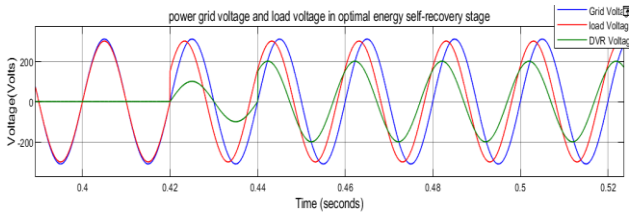

Fig.6. Initial flexible handover in optimal energy self-recovery stage.

To verify the feasibility of the MCDVR, simulations are run using MATLAB software. The system simulation model is shown in Fig.1. The MCDVR is connected in series between the supply network and the protected load.

The supply voltage is assumed to be 10kV and the source is assumed to have a reactance of 100Ω. This corresponds to a fault level of 1MVA. In the simulations, while a seven-level cascade inverter is adopted, several high-order harmonics are still present near the equivalent switching frequency. As a result, an *LC* filter should be considered in the cascaded H-bridge. If a THD of 5% is considered as a threshold for the load voltage, the proposed method can meet the requirement. Moreover, the seven-level cascade inverter can successfully ride-through both balanced and unbalanced faults for voltage dips down to 80% at the converter terminals for 243 ms.

Fig.7. shows the performance of the MCDVR under voltage sags and faults. As shown in Fig 9(a), a voltage sag occurs between 1.05s and 1.15s with a depth of 20%. In Fig 9(b), it is observed that the load voltage *U*L is regulated to a constant amplitude during this voltage sag. The system is then subjected to a three-phase downstream fault by grounding the three-phase supply for 0.1s (i.e. five cycles). The load side voltage is nearly zero during the fault (from 1.2s to 1.3s), as almost all the voltage would drop across the current-limiting module as shown in Fig. 7(b)-(c). The load current will be quickly limited to the desired value due to the current-limiting function as shown in Fig. 7(d).

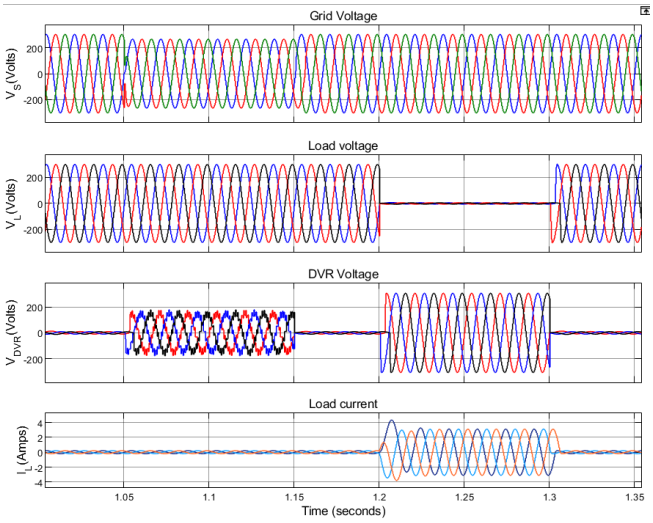

Fig.7. Simulation results of the MCDVR system. Top to bottom: (a) the supply voltage *U*s, (b) the load voltage *U*L, (c) the secondary voltage *U*dvr, (d) the load current *I*L, and (e) the dc-link voltage.

V. CONCLUSION

In this project, the adaptive schemes improve the voltage quality of sensitive loads by protecting them during grid voltage sags with phase angle jump. The optimized energy self-recovery strategy recovers the DC link voltage and mitigate the phase jump in energy self-recovery stage as well. Cascaded multilevel inverters have been applied in the industry as a cost-effective means of series sag compensation.

However, a large current will be induced into the VSI through a series transformer during faults, and this is harmful to the VSI and the other equipment in the grid. The DVR system was proposed to deal with voltage sags and short-circuit current faults. The DVR system has not only the advantages of the H-bridge cascade inverter, but also reduces the secondary side current in the preliminary period of the fault. A mathematical model of this system was also established in this project. A careful analysis of the transient state verified the feasibility of the proposed MCDVR. Additionally, based on the theoretical analysis and simulations results, we can conclude that, the proposed control method can limit fault current with two cycle.

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